

What is claimed is:

- 1 1. An output stage for a differential amplifier comprising:
2 first and second P-type input amplifiers to receive a non-inverted differential voltage
3 signal and an inverted differential voltage, respectively;
4 first and second N-type input amplifiers to receive the non-inverted differential voltage
5 signal and the inverted differential voltage, respectively;
6 a first output amplifier to receive the output of the first P-type input amplifier via an N-
7 type load and the output of the first N-type amplifier via a P-type load; and
8 a second output amplifier to receive the output of the second P-type input amplifier via an
9 N-type load and the output of the second N-type amplifier via a P-type load.
1 2. The output stage of claim 1 wherein an output voltage signal is to be provided between
2 said first and second output amplifiers.
1 3. The output stage of claim 2 wherein said first output amplifier is a P-type amplifier and
2 said second output amplifier is an N-type amplifier.
1 4. The output stage of claim 1 wherein said non-inverted differential voltage signal and said
2 inverted differential voltage signal have matched currents.
1 5. An output stage for a differential amplifier comprising:
2 first and second P-type transistors to receive a non-inverted differential voltage and an
3 inverted differential voltage, respectively;

4 first and second N-type transistors to receive the non-inverted differential voltage and the
5 inverted differential voltage, respectively;
6 a first output amplifier to receive the output of the first P-type transistor via an N-type
7 load and the output of the first N-type transistor via an N-type load; and
8 a second output amplifier to receive the output of the second P-type transistor via an N-
9 type load and the output of the second N-type transistor via an N-type load.

1 6. The output stage of claim 5 wherein an output voltage is to be provided between said first
2 and second output amplifiers.

1 7. The output stage of claim 6 wherein said first output amplifier is a P-type transistor and
2 said second output amplifier is an N-type transistor.

1 8. The output stage of claim 5 wherein said non-inverted differential voltage signal and said
2 inverted differential voltage signal have matched currents.

1 9. An output stage for a differential amplifier comprising:

2 first and second P-type transistors to receive a non-inverted differential voltage and an
3 inverted differential voltage, respectively;

4 first and second N-type transistors to receive the non-inverted differential voltage and the
5 inverted differential voltage, respectively;

6 first and second N-type loads coupled to said first and second P-type transistors,
7 respectively;

8 first and second P-type loads coupled to said first and second N-type transistors,
9 respectively;
10 first and second intermediate transistors coupled to said first P-type transistor and said
11 first N-type transistor;
12 a first output amplifier to receive the output of the first intermediary transistor and the
13 output of the second N-type transistor; and
14 a second output amplifier to receive the output of the second intermediary transistor and
15 the output of the second P-type transistor.

1 10. The output stage of claim 9 wherein an output voltage is to be provided between said first
2 and second output amplifiers.

1 11. The output stage of claim 10 wherein said first output amplifier is a P-type transistor and
2 said second output amplifier is an N-type transistor.

1 12. The output stage of claim 11 wherein said first intermediary transistor is a P-type
2 transistor and said second intermediary transistor is an N-type transistor.

1 13. The output stage of claim 9 wherein each of said transistors is a metal-oxide-
2 semiconductor field effect transistor.

1 14. The output stage of claim 7 wherein said non-inverted differential voltage signal and said
2 inverted differential voltage signal have matched currents.

1 15. The output stage of claim 12 wherein said non-inverted differential voltage signal and
2 said inverted differential voltage signal have matched currents.

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